Remarks

The amendments

The Abstract

The *Abstract* is the abstract that was originally filed with PCT/US99/10002 and published 18 November 1999 in WO 99/59078. The *Abstract* thus adds no new matter.

Claim 18

As filed, the claim lacked an antecedent for the "plurality of I/O pins" in the claim's last clause. The claim has been amended to provide the antecedent and to better conform it to claim 14. A preferred embodiment of what is being claimed is described beginning at page 32, line 31 of the Specification and shown in FIGs. 46 and 47. The claim as amended is thus fully supported by the Specification as filed.

Traversal of the rejections

Traversal of the rejections of claims 14-16 under 35 U.S.C. 102

An examiner may make a rejection of a claim under 35 U.S.C. 102 only if the reference used to reject the claim shows every limitation of the claim. In the following, Applicants will first discuss what Applicants are claiming, will then discuss the disclosure of Hansen, and will then show why Hansen does not anticipate claims 14-16.

Applicants' claim 14

Claim 14 is Applicants' only independent claim. The claim reads as follows. To aid Examiner in understanding the claim, reference numbers from Applicants' FIGs. 2 and 3, discussed beginning at page 10, line 6 of Applicants' specification, have been added to the claim:

14. An integrated circuit (203) comprising:
a plurality of data stream inputs and/or outputs that receive and/or transmit streams of data (205(0..15));
a plurality of data stream processors (307) that process the streams of data, each data stream processor being coupled to a data stream input and/or data stream output and including
a writeable instruction memory (403) containing instructions and
a control data processor (401) that controls the data stream

processor by sequentially executing instructions from the writeable instruction memory.

The claim is straightforward, but Applicants believe that it is worth noting at this point that claim is drawn to an *integrated circuit*, that the integrated circuit comprises *a plurality* of data stream processors, and that *each* data stream processor includes a writeable instruction memory and a control data processor.

What Hansen discloses

The following portion of Hansen's *Abstract* gives a good overview of the part of Hansen's disclosure which is relevant to the present context:

> A general purpose, programmable media processor for processing and transmitting a media data stream of audio, video, radio, graphics, encryption, authentication, and networking information in real-time. The media processor incorporates an execution unit that maintains substantially peak data throughout of media data streams. The execution unit includes a dynamically partitionable multi-precision arithmetic unit, programmable switch and programmable extended mathematical element. A high bandwidth external interface supplies media data streams at substantially peak rates to a general purpose register file and the multi-precision execution unit. A memory management unit, and instruction and data cache/buffers are also provided. High bandwidth memory controllers are linked in series to provide a memory channel to the general purpose, programmable media processor.

FIG. 7, described beginning at col. 11, line 56, provides an overview of Hansen's media processor. An execution unit 100, which contains an ALU, a programmable switch, and a register file, is connected to memory consisting of an instruction and buffer cache 118, ETLB and tags 122, and data buffer cache 120. The memory is in turn connected to high bandwidth interfaces 124, shown in detail in FIG. 13 and discussed in detail beginning at col. 18, line 41. As stated at col. 18. lines 44-49,

> As part of the high bandwidth interface 124, the general purpose media processor 12 integrates several fast communication channels 156 (FIG. 13) to communicate externally. These fast communication channels 156 preferably couple to external caches 150, which serve as a buffer to memory interfaces 152 coupled to standard memory 154. The caches 150 preferably comprise synchronous static random access memory ("SRAM"), each of which are sixty-four kilobytes in size; and the standard memories 154 comprise DRAM's. The memory interfaces 152 transmit

> data between the caches 150 and the standard memories 154. The standard memories 154 together form the main external memory for the general purpose media processor 12. The cache 150, memory interface 152, standard memory 154 and input/output channel 156 therefore make up a single external memory unit 158 for the general purpose media processor 12.

Hansen sets forth at col. 27, lines 20-25 that the system shown in FIG. 7 may be implemented in any manner ranging from a number of integrated circuits through an implementation using discrete circuit elements. The implementation employed in a preferred embodiment is shown in FIG. 19 and described beginning at col. 26, line 53. As set forth there, components 100, 118, 120, and 122 of FIG. 7 are implemented in a first integrated circuit labeled PROCESSOR, high bandwidth interfaces 124 are implemented in a second integrated circuit labeled MEMORY, the data stream interfaces 128 and 130 are implemented in a third integrated circuit labeled I/O, and an interface to a switch, which is apparently not shown in FIG. 7, is implemented in a fourth integrated circuit labeled SWITCH. The MEMORY, SWITCH, and I/O integrated circuits communicate with each other by means of 1 Ghz byte channel 156 in high bandwith interface 124 and execution processor 100 reads data from and writes data to the MEMORY integrated circuit and ultimately to and from the external DRAMS 154 connected thereto.

Why Hansen does not anticipate claim 14

It will be immediately apparent from the foregoing discussion of Hansen that all of the implementations which Hansen envisions of his general-purpose programmable media processor have only a *single* execution unit 100. Since there is nothing else in Hansen that corresponds in any way whatever to Applicants' "data stream processors", Hansen does not disclose claim 14's "plurality of data stream processors" and therefore cannot anticipate claim 14. Further, claim 14 requires that the "data stream processors [process] the streams of data" As shown by Applicants' FIGs 3, 4, 10, and 13, Applicants' data stream processors do indeed process the data streams as they are received from and/or output to the "data stream inputs and/or outputs" of Applicants' claim. Hansen's FIG. 2, by contrast makes it clear that Hansen's execution unit 100, by contrast, does not process

the data streams themselves, but instead processes data that has been extracted from the data steams and loaded into the external memory 154. For that reason as well, Hansen cannot anticipate Applicants' claim 14.

The differences between Hansen's general-purpose programmable media processor and Applicants' integrated circuit are not merely a matter of designer's choice or of degree of integration: Because Applicants' integrated circuit has a plurality of data stream processors, the data streams can be truly processed in parallel; in Hansen's processor by contrast, execution unit 100 can process only a single piece of a single data stream at any one time. Further, in Hansen's system, no processing can be done on any part of a data stream until the part has been copied into external memory. In Applicants' system, the data stream processors do their work on the data streams as they *pass through* the data stream processors. Because the work is done in this fashion, the data stream processor extracts all the information needed to route and format the data stream *before* the data stream is stored in buffer memory 229, and consequently, all that needs to be stored in buffer memory 229 is the stream's payload data. The extraction of the protocol data from the data stream as it passes through also permits time-critical work such as routing to be done in parallel with the storage of the data stream in buffer memory 229. Finally, since the data stream as stored in buffer memory 229 contains only payload data, transmitting the data stream simply becomes a matter of fetching the payload data from buffer memory 229 and using the data stream processor to add the protocol data required for the new routing of the payload data as the payload data passes through the data stream processor.

Dependent claims 15 and 16

Since Hansen does not anticipate claim 14, it also cannot anticipate these claims; however, even if Hansen did anticipate claim 14, it would not anticipate claim 15, which is thus patentable in its own right over Hansen. Claim 15 adds the limitation that "the control processor is a general-purpose microprocessor that has an industry-standard architecture." Hansen's execution unit is described as follows at col. 15, lines 9-12:

> The presently preferred embodiment of the general purpose media processor 12 includes a limited instruction set similar to those seen in Reduced Instruction Set Computer ("RISC") systems.

There is no indication whatever here that the general purpose media processor 12 "has an industry-standard architecture", as required by the claim, and the table of operation codes at Hansen's columns 13 and 14 makes it abundantly clear that general purpose media processor 12 does not have an industry-standard architecture but has instead been strongly specialized for media processing. The reason why the use of an industry-standard architecture here is not merely a matter of design choice is given in claim 14's whereby clause. The more programmable a device is, the more important the costs of programming the device becomes, and the more important it is that standard tools may be used to program the device.

Traversal of the rejections of claims 17-23 under 35 U.S.C. 103

These claims are all dependent either directly or indirectly from claim 14 and the rejections all involve combinations of other references with Hansen, and consequently, if Hansen does not show all of the limitations of claim 14, combinations of Hansen with other references cannot show all of the limitations of any of the claims being rejected under 35 U.S.C. 103 and Examiner has not made the *prima facie* case required for a rejection under 35 U.S.C. for any of these claims. Additionally, however, the additional references often do not show the limitation added in the dependent claim, and in these cases, the dependent claim is patentable in its own right over the combination of references.

<u>The rejection of claim 17</u>

Claim 17 adds the limitation of "an aggregator that aggregates certain of the data stream processors so that the aggregated data stream processors cooperate in processing a stream of data". Further limitations set forth components of the aggregator including "a writeable configurator that specifies the configurable interconnections and the configurable operation coordinator as required to aggregate the data stream processors". As shown in FIG. 3 and described beginning at col. 8,line 34, Kochinsky discloses a

Virtual Processor Module 130 which is made up of four dynamically programmable processing elements 1, 7, 11, and 15 operating under control of VPM controller 30, which includes a microprocessor. VPM controller 30 can reconfigure the dynamically programmable processing elements and their interconnections to do the kind of processing required for a particular task and then control VPM 130 as it performs the task, in effect making VPM 130 into a special-purpose processor for the task.

In making his rejection, Examiner cites col. 6, line 63-col. 7 line 8 and col. 8, lines 19-32. The first cited location merely sets forth that the VPM is configurable. The second cited location sets forth the efficiency advantages of the VPM. In terms of what Kochinsky discloses, the difficulty with the rejection is that Kochinsky's VPM 130 discloses at most an equivalent of a single one of Applicants' "data stream processors", as can be seen by the fact that VPM controller 30, which has a function similar to that of Applicants' control data processor, controls the entire VPM 130. Applicants' claim, however, requires "an aggregator that aggregates certain of the data stream processors". Since VPM 130 is equivalent to at most one of Applicants' data stream processors, Kochinsky cannot and does not disclose the aggregator of claim 17. Claim 17 is thus patentable not only because it is dependent from claim 14, but also in its own right over Hansen and Kochinsky.

The rejection of claim 18

The added limitations of claim 18 are addressed to the feature of Applicants' invention that a data stream input and/or output may be used with a number of different transmission protocols and may be dynamically reconfigured to be used with particular ones of the transmission protocols. Examiner cites Murata in rejecting the claim, but as set forth in the *Abstract,* Murata deals with arrangements for dynamically upgrading the programs being used in a disk controller while the controller is operating. None of this appears to have anything whatever to do with Applicants' claimed technique for configuring a data stream input and/or output for a particular transmission protocol. Examiner cites col. 10, lines 19-34 of Murata in his rejection, but the cited location sets forth the criteria by which the bits in "executable processor designation bit map 821" are

set. Bitmap 821 is shown in FIG. 4. Since Murata is simply not relevant to the added limitations of claim 18, claim 18 is patentable in its own right over Hansen and Murata.

The rejection of claim 19

Claim 19 adds the limitation that each data stream processor further comprises a receive processor and an transmit processor, both of which operate under control of the control data processor. Examiner cites Deb in rejecting the claim and Deb in fact discloses a system which includes a transmit stream processor and a receive stream processor. Claim 19 requires, however, that the claim's receive processor and transmit processor operate under control of the control data processor. Deb's FIG. 8, which Examiner cites in his rejection, shows nothing equivalent to Applicants' control data processor, and col. 21, lines 30-67 cited by Examiner makes no mention of anything equivalent to Applicants' control data processor. Deb's FIG. 2A, which provides a more detailed view of Deb's system, also shows nothing equivalent to Applicants' control data processor. In particular, as pointed out at col. 9, lines 8-17 of Deb, μrisc stream processor 114(c) does not control μrisc stream processors 114(a) and (b), but merely indicates to those processors that events have occurred in controllers 118 and 120. Because nothing in Deb shows anything equivalent to the control of the transmit stream processor and receive stream processor set forth in the added limitation of claim 19, claim 19 is also patentable in its own right over Hansen and Dev.

The rejections of claims 20 and 21

These claims are dependent from claim 19 and are therefore patentable for that reason. For the added limitations of these claims, Examiner again refers Applicants to Hansen. In claim 20, the added limitation is that each of the receive and transmit processors includes a writeable instruction memory containing instructions to be executed by the receive and transmit processors. The difficulty with the rejection is that Hansen discloses only a single processor with a writable instruction memory, namely execution unit 100, while what the claim requires is a configuration including the control data processor, a receive processor and a transmit processor, and it is these latter processors which are required to have writeable instruction memory in the claim. Since Hansen does not

disclose the added limitation, claim 20 is also patentable in its own right over Hansen and Deb.

With regard to claim 21, the added limitation is that the receive processor and the transmit processor are configurable to bypass components of the processors during processing. Here, Examiner refers Applicants to FIGs. 5 and 6, which are high-level block diagrams of various systems, and to col. 11, lines 24-32, which merely states that "the general purpose media processor 12 is dynamically partitionable to allocate the appropriate amount of processing for each combination of media in a unified media data stream". As indicated above, Hansen's media processor does not process the stream as it is received or transmitted, but rather after it has been received and stored in memory or before it is transmitted. Anything corresponding to what is set forth in Applicants' claims would have to be done in blocks 126 and 128 of Hansen's system, about which there is essentially no disclosure in the reference. Claim 21 is thus patentable in its own right over Hansen and Deb.

The rejections of claims 22 and 23

These claims are multiply-dependent from claims 14-21. The additional limitation of claim 22 is a context processor, which Examiner believes he has found in Yajima. As set forth in Yajima's Abstract, Yajima's system is a system for encoding and decoding image data. Examiner bases his rejection on col. 5, lines 41-49:

> More specifically, as each pixel datum forming the image data stream is sent to the arithmetic encoder means of the presently preferred embodiments, it is initially received by the context generator and encoder processor. The context generator generates the reference pixel data for the present pixel datum from portions of the image data stream already received and relays it to the index generator formatted as the context signal CX.

As is apparent from the foregoing, what is meant here by "context" is information about past encoded pixels which determines how the present pixel will be encoded. In the terms used in Applicants' patent application, Yajima's context is obtained from the payload of the incoming data stream and is used to encode the incoming data stream.

"context" as the term is employed in Applicants' patent application has nothing to do with "context" as the term is employed in Yajima. Examples of what is meant by "context information" in Applicants' patent application are given at page 59, line 20 through page 60, line 30. The examples include the information needed to do address translation, the information needed to compute a CRC for a packet, and statistics concerning the packet stream. "Context information" is thus information about the packet that is not part of the packet's payload. It is precisely because the context information is not part of the payload that it can be sent off to the context processor (TLE 301) to be processed by TLE 301 as the data stream processor works on DMA'ing the payload to buffer memory 229. Because "context" as used in Yajima has nothing to do with "context" as used in Applicants' Specification and claims, Yajima cannot supply the added limitations of claim 22 and the claim is patentable in its own right over the references under which it is rejected.

The additional limitations of claim 23 are concerned with the arrangements in Applicant's integrated circuit for buffering payload in buffer memory 229 and using queues of descriptors including buffer tags specifying buffers in buffer memory 229 to manage transmission of payloads from buffer memory 229. The arrangements include buffer manager 315 and queue manager 305. Examiner finds these additional limitations in FIG. 2A of Deb. In Examiner's reading of FIG. 2A onto claim 23's additional limitations, FIFO controllers 110, 112 correspond to Applicants' buffer manager and queue FIFO 106, 108 correspond to Applicants' queue manager. The greatest difficulty with this reading is that Applicants' queues contain "descriptors of payload", while as indicated by the names of FIFOs 106, 108, they contain packets, not "descriptors of payload". What Applicants' claim language regarding the queue manager sets forth is a consequence of an important distinction between Applicants' invention and Deb. In Deb, information that would be stored in descriptors in Applicants' system is stored in the data structures shown in Deb's FIGs. 5A-5D and these data structures are appended to the leading edges of Deb's packets, as shown in FIGs. 5E, 6, and 7. What is stored in FIFOs 106, 108 is packets with their appended data structures. Applicants' system, by contrast, *separates* its descriptors from the packet payload, with the packet payload going to

buffer memory 229 and the descriptors going to queues managed by queue manager 305. This separation has important of advantages:

- it makes it possible to store only the payload from the packet in buffer memory 229, which greatly simplifies changing the kind of packet used to carry the payload;
- routing and scheduling can be done by manipulating the relatively small descriptors instead of the packets they represent.

For example, in Deb's system, the process of receiving a packet at 141 and then outputting it at 140 involves first storing the entire packet in FIFO 108 and then, at the proper time, moving the entire packet to FIFO 106. In Applicant's system, the payload is stored in buffer memory 229 and the descriptor for the payload is placed on a queue for a stream processor. When the descriptor reaches the head of the stream processor's queue, the steam processor fetches the payload from buffer memory 229 and outputs it.

Because Deb stores the data structures for the information about the packet with the packet, there is nothing also nothing in Deb corresponding to the behavior of the buffer manager set forth in claim 23: namely that the buffer manager responds to a write operation that writes payload to buffer memory 229 with a buffer address for the payload that has been written. This buffer address is of course part of the descriptor for the payload.

Since Deb does not disclose the added limitations of Applicants' claim 23, that claim, too, is patentable in its own right over the references employed by Examiner to reject it.

Conclusion

Applicants have provided Examiner with a copy of the Abstract as originally filed with the PCT application and have traversed all of Examiner's rejections, and have thereby been completely responsive to Examiner's first Office action of 6/28/04. Applicants have further amended their claim 18 to provide an antecedent and to better conform the claim to claim 14 from which it is dependent and have demonstrated that the claim as amended is fully supported by the Specification as filed. Applicants have thereby fulfilled the requirements of 37 C.F.R. 1.116(b) and respectfully request that Examiner

continue with his examination of the application as provided by 37 C.F.R. 1.116(a). No fees are believed to be required by reason of this amendment; should any be, please charge them to deposit account number 501315.

Respectfully submitted,

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